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Claims

[c1] A method of forming a buried collar on a sidewall of a trench in a semiconductor substrate comprising:
(a) providing said trench in said semiconductor substrate, said trench having a first dielectric layer formed on said sidewall in a upper region of said trench and a conductive material filling a lower region of said trench and a portion of said upper region of said trench, said conductive material covering a lower portion of said first dielectric layer;
(b) removing said first dielectric layer not covered by said conductive material whereby a portion of said sidewall in said upper region is exposed;
(c) forming a second dielectric layer on said exposed sidewall of said upper region and on a top surface of said conductive material;
(d) removing an uppermost portion of said second dielectric layer from said sidewall in said upper region;
(e) forming a third dielectric layer on said exposed sidewall of said upper region; and
(f) increasing the thickness of said second dielectric layer to form said buried collar.

[c2] The method of claim 1, further including:
(g) removing said second dielectric layer from said top surface of said conductive material; and
(h) filling said upper region with an additional conductive material.

[c3] The method of claim 1, wherein step (d) includes in the order recited:
filling said trench with a spin-on material; and
removing an upper portion of said spin-on-material.

[c4] The method of claim 1, wherein step (c) includes performing a thermal oxidation process, forming a high temperature oxide on said exposed sidewall or depositing an oxide on said exposed sidewall.

[c5] The method of claim 1, wherein step (e) includes performing a nitridation process to form said third dielectric layer.

[c6] The method of claim 1, wherein said first dielectric layer comprises silicon nitride, said second dielectric layer comprises silicon oxide, said third dielectric layer comprises silicon nitride and said conductive material is comprised of polysilicon.

[c7] The method of claim 1, wherein said collar is 200 to 400 Å thick and said trench is 1000 Åor less in diameter.

[c8] The method of claim 1, further including:
before step (a) forming a doped region in said semiconductor substrate, said doped region surrounding said lower region of said trench and forming a fourth dielectric layer on said sidewall of said trench in said lower region of said trench; and
before step (b) doping said conductive material by diffusion from said doped region through said fourth dielectric layer into said conductive material.

[c9] The method of claim 1, wherein said lower region of said trench is wider than said upper region of said trench.

[c10] The method of claim 1, further including forming a vertical transistor in said trench above said buried collar.

[c11] A method of forming a buried collar on a sidewall of a trench in a semiconductor substrate comprising:
(a) providing said trench in said semiconductor substrate, said trench having a first dielectric layer formed on said sidewall in an upper region of said trench and a conductive material filling a lower region of said trench and a portion of said upper region of said trench, said conductive material covering a lower portion of said first dielectric layer;
(b) forming an amorphous silicon layer on said first di-

electric material and on a top surface of said conductive material;

(c) forming a second dielectric layer on said amorphous silicon layer;

(d) removing an uppermost portion of said second dielectric layer leaving an exposed portion said amorphous silicon layer in said upper region;

(e) forming a third dielectric layer on said exposed portion of said amorphous silicon layer;

(f) removing said second dielectric layer, said amorphous silicon layer and said first dielectric layer where said amorphous silicon layer is not covered by said third dielectric layer whereby a portion of said sidewall in said upper region is exposed; and

(g) forming said buried collar on said exposed sidewall.

[c12] The method of claim 11, further including:

(h) removing an oxide layer formed on a top surface of said conductive material during step (g); and

(i) filling said upper region with an additional conductive material.

[c13] The method of claim 11, wherein step (d) includes in the order recited:

filling said trench with a spin-on material; and

removing an upper portion of said spin-on-material.

[c14] The method of claim 11, wherein step (c) includes performing a thermal oxidation process to form said second dielectric on said exposed portion of said amorphous silicon layer.

[c15] The method of claim 11, where in step (g) includes performing a dry oxidation to form said buried collar on said exposed sidewall.

[c16] The method of claim 11, wherein said first dielectric layer comprises silicon nitride, said second dielectric layer comprises silicon nitride, said third dielectric comprises silicon oxide and said conductive material comprises polysilicon.

[c17] The method of claim 11, wherein said collar is 200 to 400 Å thick and said trench is 1000 Å or less in diameter.

[c18] The method of claim 11, further including:
before step (a) forming a doped region in said semiconductor substrate, said doped region surrounding said lower region of said trench and forming a fourth dielectric layer on said sidewall in said lower region; and
before step (b) doping said conductive material by diffusion from said doped region through said fourth dielectric layer into said conductive material.

[c19] The method of claim 11, wherein said lower region of said trench is wider than said upper region of said trench.

[c20] The method of claim 11, further including forming a vertical transistor in said trench above said buried collar.